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PATENT APPLICATION

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OPTIMIZED CONDUCTIVE LID MOUNTING FOR INTEGRATED CIRCUIT CHIP CARRIERS

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Commissioner For Patents
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Alexandria, VA 22313-1450

Sir:

Applicants are hereby submitting certified copy of the foreign application, OPTIMIZED CONDUCTIVE LID MOUNTING FOR INTEGRATED CIRCUIT CHIP CARRIERS , Patent Application # 03368007.5 filed on 30 JAN 2003, as specified in 35 U.S.C. § 119(b).

Respectfully submitted,

Date: 28 August 2006

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The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

03368007.5

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
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Demande no:

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Optimized lid mounting for electronic device carriers

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
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Internationale Patentklassifikation/International Patent Classification/
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PT SE SI SK TR LI

OPTIMIZED LID MOUNTING FOR ELECTRONIC DEVICE CARRIERS

Field of the Invention

The present invention relates generally to semiconductor packaging and more specifically to simplified lid mounting of electronic device carriers, optimizing thermal dissipation and electromagnetic interference shielding.

Background of the Invention

Integrated circuits (IC) are formed on semiconductor dies, most commonly made of silicon. For handling convenience, ease of use, and reliability, the dies are often encapsulated in a protective mold material. The mold material can be ceramic, plastic, or resin. To provide an electrical interface to an IC's signal, power, and ground lines, the IC package includes an electrical connector extending from the integrated circuit to the outside of the package.

One IC package type known to those skilled in the art of IC package design is a Pin Grid Array (PGA) package. In a PGA, a plurality of pins extend from the undersurface of the package to the outside. The pins provide an electrical interface between the IC package and external circuitry. They are arranged in multiple rows and columns.

A Ball Grid Array (BGA) package is similar to a PGA package. The difference between the two is, that in a BGA

package, conductive spheres replace the pins used in a PGA package. The conductive spheres are often solder balls.

Use of the conductive spheres as an electrical interface between the package and the external circuitry permits surface mounting of the BGA package. The package is placed on a Printed Circuit Board (PCB), with the conductive spheres positioned on top of the PCB's pads. For every conductive sphere there is a corresponding pad on the board. The spheres are then soldered to the pads.

One fundamental advantage of the grid array-based IC packages, such as BGA, is that they allow high density interconnects between the ICs and the printed circuit boards on which the ICs are eventually installed. The high density interconnects, i.e., high lead densities and counts, result from using all or a portion of the area of a surface of the IC for multiple rows and columns of the electrical interface. The increased area utilization in grid array package allows chip designers to place more leads in a given package size.

High lead counts on BGA packages are needed to support high and constantly increasing IC circuit densities. High circuit densities combined with the increase of signal frequency tend to aggravate the problems of heat dissipation, electromagnetic interference and electromagnetic susceptibility.

To cope with heat dissipation, the lid, often being made of Copper and used as a stiffener and heat spreader, is generally mounted on top of the integrated circuit using a thermally conductive material. Generally, the lid is not electrically connected to any electrical potential, leaving

this Copper piece "floating". Figure 1 illustrates how a lid is generally mounted on top of an integrated circuit, or chip, in a standard IC package 100. In this example, chip to chip carrier interconnection is performed with Controlled Collapse Chip Connection (IBM C4 technology), widely known as Flip-Chip Attach (FCA). Such technology provides high I/O density, uniform chip power distribution, high cooling capability and high reliability. Therefore, chip 110 is electrically connected to multi-layer chip carrier 120 using C4 solder balls 130. The cavity formed between chip 110 and chip carrier 120 is underfilled with dielectric material such as epoxy to reinforce the chip to chip carrier electrical interconnection. Chip carrier 120 is electrically connected to a PCB (not represented for sake of clarity) with BGA solder balls 150, as described above. Lid 160, being used for heat dissipation is thermally connected and bonded to chip 110 with thermal adhesive 170. On the external side of the package, the lid may be maintained with a piece 180, generally made of dielectric material, also used as a stiffener. Or like in the case of the IBM process called Direct Lid Attachment (DLA), the lid is attached directly to the back side of the Silicon and left overhanging the chip with no stiffener placed onto the laminate.

In order to overcome the EMI problem, the conductive lid may be grounded by replacing the conventional electrically nonconductive adhesive for attaching the lid to the chip carrier with an electrically conductive adhesive. For example, an electrically conductive thermosetting silicone adhesive or a solder may be used as the electrically conductive adhesive.

The electrically conductive thermosetting silicone adhesive performs the buffer function for reducing the

stresses between the lid and the chip carrier, generated by difference of the Coefficient of Thermal Expansion of the different materials joined and or bonded together. However, the electrically conductive thermosetting silicone adhesive does not produce good adhesion between the chip carrier and the lid. In contrast, the solder would provide an excellent mechanical attachment between the chip carrier and the lid. However, the solder does not perform well as the stress buffer. That is, when solder is used, cracks or delaminations may be caused at the interface between the lid and the chip carrier due to thermal stresses. Such cracks can degrade the heat removal capacity of the package and further degrade electrical performance of the chip. It is recognized that development effort for finding the right electrical and thermal conductive material providing required mechanical properties is going to be a very long lead effort.

Further, it is difficult for a paste adhesive or solder to bridge the gap between the bottom surface of the lid and top surface of the chip carrier which is typically at least 0.7mm since it would require a large pad area. This large pad area is needed to accommodate a quantity of material that has to be sufficient not only to effectively fill the gap between the laminate and the lid but, the material quantity also needs to have the right size and properties to guarantee that, when the lid is placed in contact with the dispensed material, the lid surface will be wetted by the material. Without a good wetting of the lid surface it is difficult to achieve a reliable bond.

To handle practically and efficiently EMI shielding, US Patent Application n°2002/0113306 discloses a semiconductor package with a lid handling the function of a Faraday cage. As illustrated on Figure 2, the integrated circuit package

200 includes a substrate or chip carrier 210, a chip 220 having bound pads 230, a lid 240 attached on the upper surface of the substrate so as to cover the chip and one or more projections 250 that electrically connect the lid 240 to a plurality of ground patterns. The substrate has substrate pads formed on the upper surface, and one or more of the substrate pads extend to form the ground patterns. The chip 220 is bonded on the upper surface of the substrate 210. One or more of the bond pads are ground bond pads, and the bond pads are electrically connected to the corresponding substrate pads. An electrically nonconductive adhesive 260 is used for the attachment of the lid 240 to the substrate 210, and the projections 250 are connected to the ground patterns by an electrically conductive adhesive 270. The ground projections are positioned at four corners of a cavity that is formed between the substrate 210 and the lid 240. The semiconductor package 200 further includes a thermal interface material 280, interposed between lid 240 and the chip 220, the thermal interface material 280 transmitting heat generated by the chip 220 to the lid 210.

However such based solutions present drawbacks that generally add significant time and cost in manufacturing assembly. Firstly, as illustrated on Figure 3, the lid with its projections must be positioned precisely to avoid any electrical short. Figure 3 represents a partial plan view of the upper surface of the substrate 300 wherein semiconductor chip 310 is positioned. Since the size of the substrate pads 320 connected to the ground patterns, wherein lid projections are connected, is very small when compared to the size of the lid, such precision positioning requires adapted manufacturing tools for alignment and result in higher cycle time for placement. Circle 330 represents lid projection positions leading to electrical shorts between ground and

signal tracks. Likewise, due to its nature and the low volume to be applied, the conductive adhesive material must be precisely positioned and dispensed. Furthermore, the manufacturing process may be complex since, for example, different adhesive materials are used simultaneously and in close proximity which could lead to intimate contact between these adhesives.

Summary of the Invention

Thus, it is a broad object of the invention to remedy the shortcomings of the prior art as described here above.

It is another object of the invention to provide an optimized lid mounting for electronic device carriers, using standard manufacturing process steps of semiconductor packaging.

It is a further object of the invention to provide an optimized lid mounting for electronic device carriers, optimizing heat dissipation and electromagnetic interference shielding.

It is still a further object of the invention to provide an optimized lid mounting for electronic device carriers, leaving the lid electrically floating but creating thermally enhanced dissipation paths between the lid and the laminate chip carrier features, like power planes and the Ball Grid Array footprints.

The accomplishment of these and other related objects is achieved by a semiconductor package comprising a chip carrier including at least one grounded pad on a side, at least one semiconductor chip connected to said side of said chip carrier, a conductive lid being thermally connected to said at least one semiconductor chip and at least one conductive block, said at least one conductive block being electrically connected to said at least one grounded pad and to said conductive lid,

and a method for manufacturing a semiconductor package, comprising a chip carrier having at least one grounded pad, said method comprising the steps of:

- dispensing a first electrically conductive adhesive material on said at least one chip carrier grounded pad;
- picking and placing at least one conductive block in contact with said electrically conductive adhesive material;
- picking and placing at least one semiconductor chip on said chip carrier;
- dispensing a second electrically conductive adhesive material on said at least one conductive block;
- dispensing electrically insulative adhesive material on said at least one semiconductor chip; and,
- placing a conductive lid in contact with said second electrically conductive adhesive material and said electrically insulative adhesive material.

Further advantages of the present invention will become apparent to the ones skilled in the art upon examination of the drawings and detailed description. It is intended that any additional advantages be incorporated herein.

Brief Description of the Drawings

Figure 1 illustrates how lids are generally mounted on top of semiconductor chips in a standard integrated circuit package.

Figure 2 shows a prior art solution of lid mounting for shielding electromagnetic interferences.

Figure 3 represents a partial plan view of the upper surface of a substrate wherein a semiconductor chip is positioned, illustrating how precisely the lid must be positioned when using solution presented on figure 2.

Figure 4 is a partial cross section view of a semiconductor package illustrating a first embodiment of the invention.

Figure 5 shows a plan view of the semiconductor package of figure 4.

Figure 6 is a partial cross section view of a semiconductor package illustrating a second embodiment of the invention.

Figure 7 , comprising figures 7a and 7b, depicts an example of how the manufacturing process flow for implementing the invention can be merged with the standard manufacturing process flow of chip packaging.

Detailed Description of the Preferred Embodiments

According to the invention there is provided a semiconductor package having a conductive lid allowing heat dissipation and electromagnetic interference shielding, this lid

being mounted with a standard manufacturing process. For sake of illustration, the description of the invention is based upon BGA/C4 semiconductor packages however, it must be understood that the invention may be implemented with most of the other semiconductor packages.

Discrete components such as chip capacitors or chip resistors, when soldered to the chip carrier surface match closely the at least 0.7mm gap between the bottom surface of the lid and top surface of the chip carrier. Therefore, the main principle of the invention consists in using conductive modules, having approximately the size of discrete components, to bridge grounded pads of the chip carrier and the conductive lid. Such conductive modules may be soldered on grounded pads and electrically connected to the conductive lid with an electrically conductive adhesive.

Figure 4 illustrates a first embodiment of the semiconductor package according to the invention. Like the semiconductor package of figure 1, the semiconductor package 100' of the invention comprises a semiconductor chip 110 positioned on a chip carrier 120' and electrically connected to signal and ground tracks of external conductive layer through C4 solder balls 130. As mentioned above, the cavity formed between chip 110 and chip carrier 120' may be underfilled with dielectric material such as epoxy to reinforce the chip to chip carrier electrical connection. Chip carrier 120' is electrically connected to a PCB (not represented for sake of clarity) with conductive BGA solder balls 150 and lid 160, being used for heat dissipation, is thermally connected and bonded to chip 110 with thermal adhesive 170.

According to the first embodiment of the invention, the conductive lid 160 is electrically connected to the ground

through a conductive block 400 that could be made, for example, of Copper. On its upper side, conductive block 400 is electrically connected to lid 160 with electrically conductive adhesive material 410 e.g., Silicone based material or similarly compliant adhesive such as low modulus epoxies, polyurethanes or acrylics. On its lower side, conductive block 400 is soldered with soldering 420, or electrically connected with electrically conductive adhesive material, to a pad 430, designed in the chip carrier 120' and connected to a ground track. Conductive block 400 may also be bonded to chip carrier 120' with non conductive adhesive material 440 to avoid any displacement during manufacturing.

The conductive block 400 can have one or two sides Ni plated for better compatibility of the adhesion properties of silicone based material. Likewise, the lid that may be made of Copper could also be Ni plated. Further, one skilled in the art will know that other surface treatment choices that provide low and stable contact resistance could be used for either the block or the lid. These choices include passivated copper, tin, tin-lead, or noble metals such as gold, silver, palladium, silver-palladium or palladium-nickel alloys.

As mentioned above the conductive block 400 has preferably the size of standard Surface Mount Technology (SMT) discrete components, commonly placed on board of chip carriers, so that manufacturing process uses the standard pick and place operation. Still in a preferred embodiment, lid 160 is electrically connected to ground tracks of chip carrier 120' through four conductive blocks 400-1 to 400-4 as illustrated on figure 5, representing a partial plan view of the semiconductor package 100'. Furthermore, even though

conductive block 400 is soldered on two different pads on figure 4, only one is required to electrically connect a ground track of chip carrier 120' to lid 160.

The copper block attached with solder joints along the laminate chip carrier side, and the electrically and thermally conductive adhesive on the lid side represent an ideal thermal dissipation path from the heat spreader (lid) to the Ground network within the laminate chip carrier enhancing the thermal dissipation properties of the electronic package. The same thermal performance benefit is achieved using a non electrically conductive resin but with specific or optimized thermal conductivity characteristics between the Copper block and the lid.

Figure 6 illustrates a second embodiment of the semiconductor package according to the invention. Semiconductor package 100" still comprises a semiconductor chip 110 positioned on a chip carrier 120' and electrically connected to signal and ground tracks of external conductive layer through C4 solder balls 130. The cavity formed between chip 110 and chip carrier 120' may be underfilled with dielectric material such as epoxy to reinforce the chip to chip carrier electrical interconnection. Likewise, chip carrier 120' is electrically connected to a PCB (not represented for sake of clarity) with conductive BGA solder balls 150 and lid 160, being used for heat dissipation is thermally connected and bonded to chip 110 with thermal adhesive 170.

According to the second embodiment of the invention, the conductive block 400 of figure 4 is replaced by a spring that could be, for example, a CuBe (Copper Beryllium alloy) spring. The spring shape of the connecting part between the lid 160 and the chip carrier 120' allows to effectively

compensate Coefficient of Thermal Expansion (CTE) mismatch between large components (lids and carriers) when a Copper lid is mounted for example on a Ceramic carriers or even with Copper lid attached to organic laminates. It must be noticed that a large beneficial effect is obtained if CuBe springs are placed along the longer diagonal of the semiconductor package as illustrated on figure 5.

As mentioned above, the invention is based upon the standard process flow, currently available on the manufacturing floor and the available process capability of the equipment set. For example, the conductive block 400 can be obtained from a metal reel and taped into embossed tapes and reeled for pick and place utilization.

The overall 90% of the gap between the carrier and the lid is covered by the conductive block or spring, leaving only a thin gap to be filled with the electrically conductive material. Dispense of the material can be done along with the same machine and the same time when the other Silicone based material is dispensed between the lid and the back side of the chip. The lid attach operation remains the same. Strain and stress build up are not of concern here due to the different properties of the conductive block if compared to the Silicone or other materials like Ceramics. CTE mismatch between lid and chip carrier or lid and semiconductor is not a concern because of the compliant property of the silicone adhesive. Soldering of the conductive block is fully compatible with the current manufacturing process flow and the resulting solder joint is mechanically stronger compared for example with adhesive posts.

Figure 7 illustrates the main steps of the manufacturing process flow used for semiconductor packaging, allowing the implementation of the invention. The bare chip carrier is manufactured according to standard design rules and process (step 700) since the only requirement for implementing the invention consists in designing pads, connected to ground tracks, at the surface layer of the chip carrier, on the lid side. Such pad design is a standard operation used e.g., for chip electrical connections. Then, during the standard step consisting in depositing solder alloy on the C4 receiving pad of the laminate chip carrier to connect the chip, solder is also deposited on chip carrier pads, where discrete components and conductive blocks linking chip carrier to lid have to be placed (step 705). After solder has been applied, discrete components and conductive blocks linking chip carrier to lid are automatically picked and placed (step 710). As mentioned above, discrete components and conductive blocks, having approximately the same size, allow the same pick and place tool to be used for both operations. Naturally, as discussed above, a dot of glue may be disposed between the chip carrier and the discrete components and conductive blocks before they are placed to avoid displacement. Likewise, semiconductor chips are picked and placed (step 715). Following these pick and place steps, a reflowing operation is performed to solder discrete components, conductive blocks linking chip carrier to lid and chips (step 720). Then, BGA solder balls are put in place, a reflowing operation is performed (step 725) and, after electrical test, the space comprised between semiconductor chip and chip carrier is underfilled with a dielectric material that is cured (step 730). Then, adhesive materials such as resins are disposed on top of the semiconductor chips and the conductive blocks linking chip carrier to lid (step 735). The adhesive material disposed on top of the

semiconductor chips is insulative while the one disposed on top of the conductive blocks linking the chip carrier to the lid is conductive. When the adhesive material is dispensed, the lid is placed and the adhesive material is cured (step 740).

While the process has been described to implement the invention according to the first embodiment wherein conductive blocks are used to link chip carrier to lid, the process to implement the second embodiment wherein conductive springs are used to link chip carrier to lid is exactly the same.

Therefore, as it can be seen from figure 7, the invention is based upon standard process flow of manufacturing semiconductor chip package, allowing an efficient heat dissipation and electromagnetic interference shielding without increasing manufacturing costs.

Naturally, SMT discrete components may be used to replace conductive blocks or springs, avoiding making adapted conductive blocks having particular features e.g., size, coefficient of thermal expansion and adhesivity. In such a case, the SMT discrete components are used only to connect chip carrier ground to the lid, they are not acting as a resistor or capcitor. Likewise, it could be possible to use other components integrating several functions, one being dedicated to electrically connect chip carrier ground to the lid and the remaining two to the original discrete component destination of electrical contact for a passive electrical component.

Naturally, in order to satisfy local and specific requirements, a person skilled in the art may apply to the solution described above many modifications and alterations all of which, however, are included within the scope of protection of the invention as defined by the following claims.

Claims:

1. A semiconductor package comprising a chip carrier including at least one grounded pad on a side, at least one semiconductor chip connected to said side of said chip carrier, a conductive lid being thermally connected to said at least one semiconductor chip and at least one conductive block, said at least one conductive block being electrically connected to said at least one grounded pad and to said conductive lid.

2. The semiconductor package of claim 1 wherein said at least one conductive block is soldered to said at least one grounded pad.

3. The semiconductor package of either claim 1 or claim 2 wherein said at least one conductive block is electrically connected to said at least one grounded pad with electrically conductive adhesive material.

4. The semiconductor package of any one of claims 1 to 3 wherein said at least one conductive block is electrically connected to said conductive lid with electrically conductive adhesive material.

5. The semiconductor package of any one of claims 1 to 4 wherein said at least one conductive block is further linked to said chip carrier using an electrically insulative adhesive material.

6. The semiconductor package of any one of claims 1 to 5 wherein said at least one conductive block is further linked to said chip carrier using an optimized thermally conductive adhesive material.

7. The semiconductor package of any one of claims 1 to 6 wherein said at least one conductive block is a conductive spring.

8. The semiconductor package of any one of claims 1 to 6 wherein said at least one conductive block is a SMT discrete component.

9. A method for manufacturing a semiconductor package, comprising a chip carrier having at least one grounded pad, said method comprising the steps of:

- dispensing a first electrically conductive adhesive material on said at least one chip carrier grounded pad;
- picking and placing at least one conductive block in contact with said electrically conductive adhesive material;
- picking and placing at least one semiconductor chip on said chip carrier;
- dispensing a second electrically conductive adhesive material on said at least one conductive block;
- dispensing electrically insulative adhesive material on said at least one semiconductor chip; and,
- placing a conductive lid in contact with said second electrically conductive adhesive material and said electrically insulative adhesive material.

10. The method of claim 9 wherein said first electrically conductive adhesive material comprises solder.

11. The method of either claim 9 or claim 10 wherein said at least one conductive block is either a conductive spring or a SMT discrete component.

OPTIMIZED LID MOUNTING FOR ELECTRONIC DEVICE CARRIERS

Abstract

An optimized lid mounting for electronic device carriers, using standard manufacturing process steps of semiconductor packaging, optimizing heat dissipation and electromagnetic interference shielding is disclosed. According to the invention, conductive blocks or springs are soldered to ground pads of the chip carrier on their lower side. On the other side, these conductive blocks or springs are electrically connected to the lid with conductive adhesive material such as silicon based material. Furthermore, the lid is thermally connected to the semiconductor chip with electrical insulative adhesive material.

Figure 6.

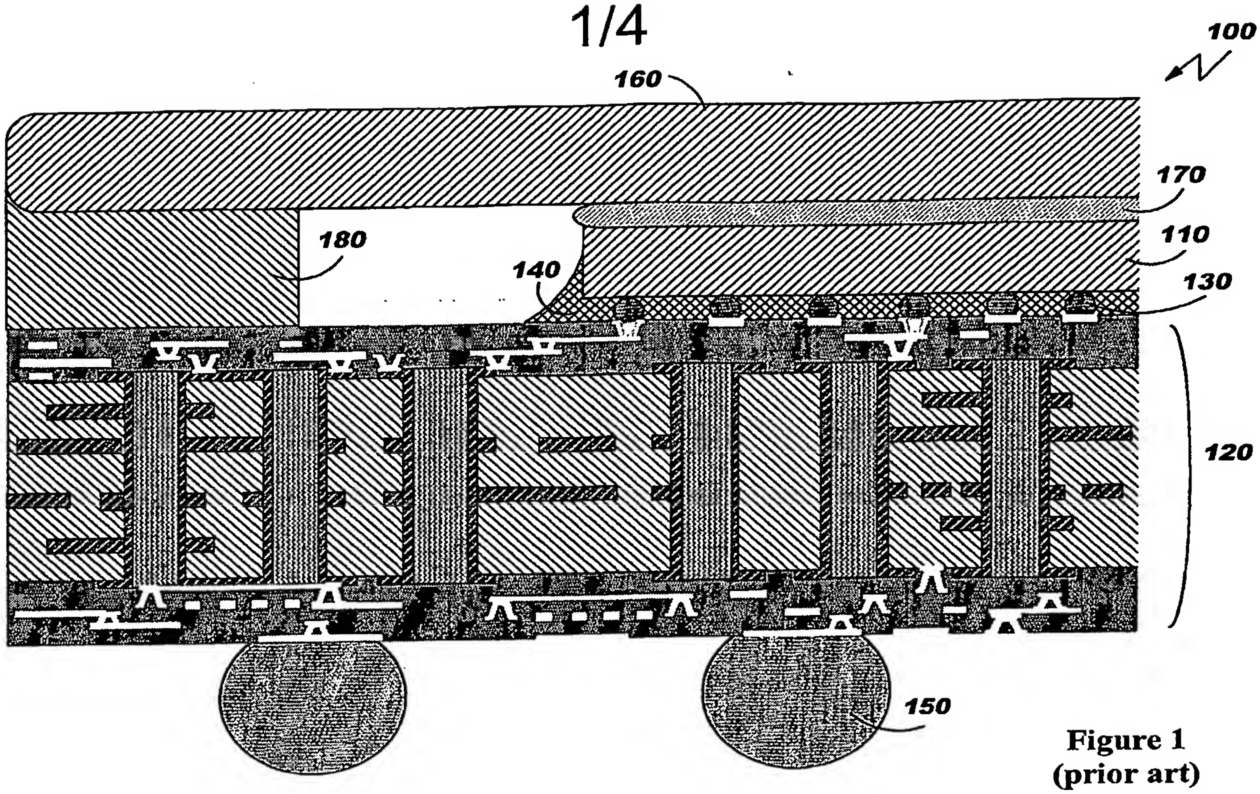

Figure 1
(prior art)

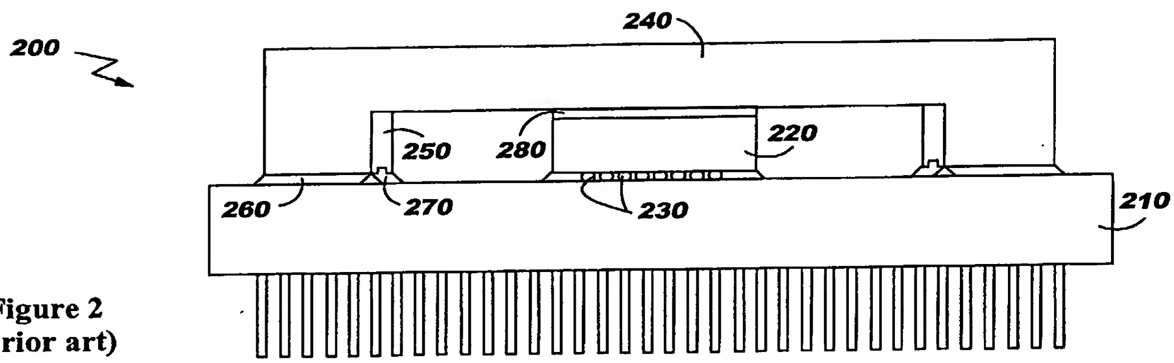

Figure 2
(prior art)

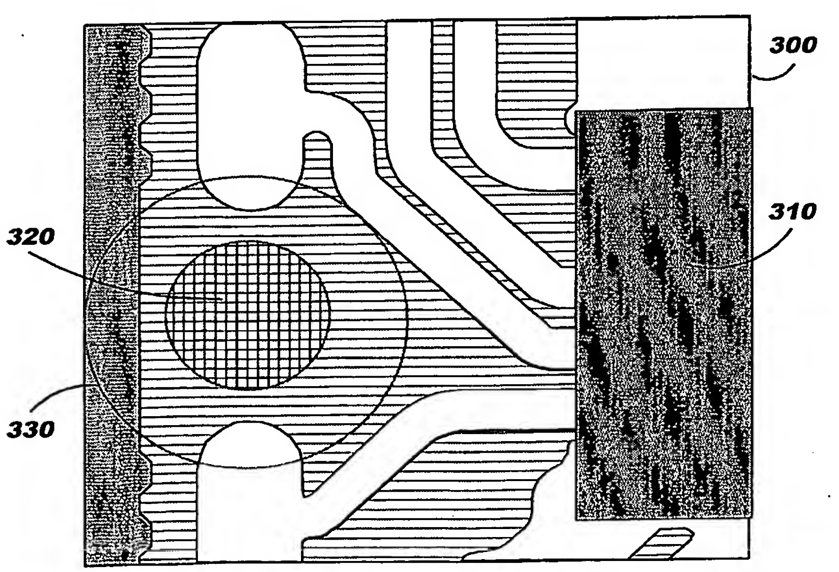

Figure 3
(prior art)

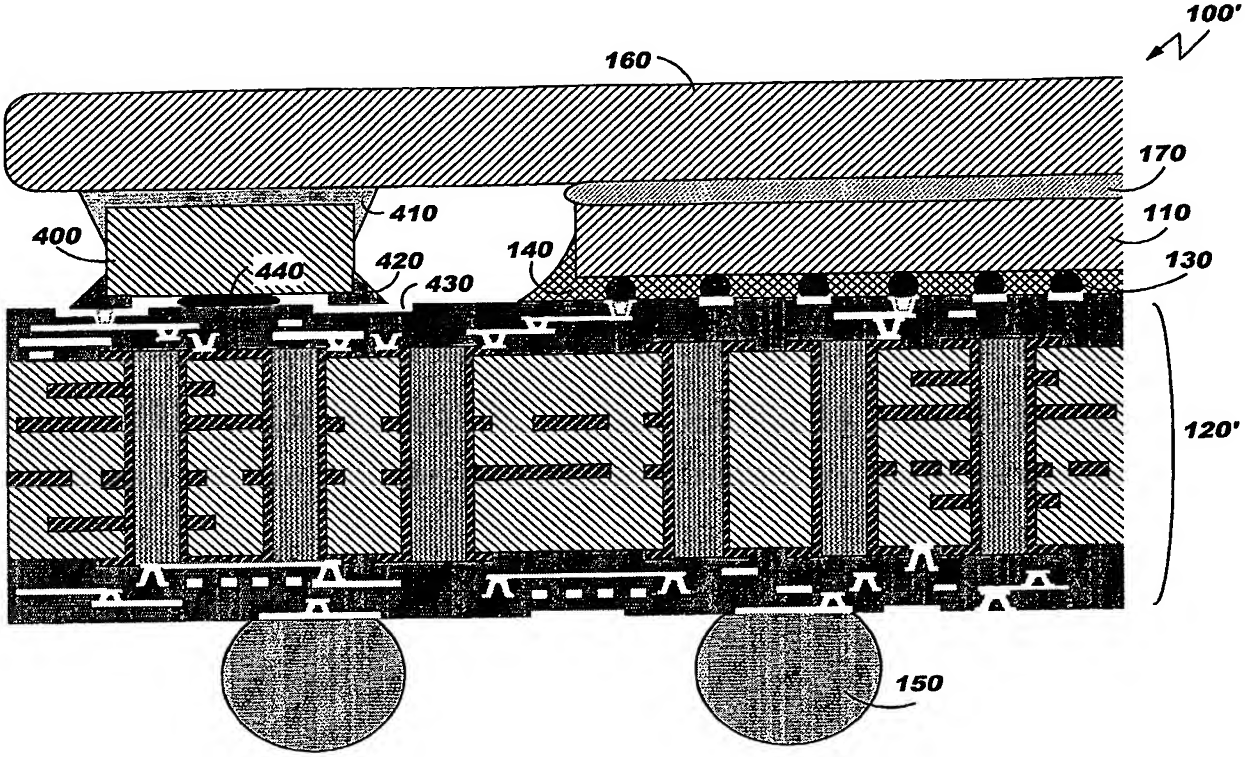

Figure 4

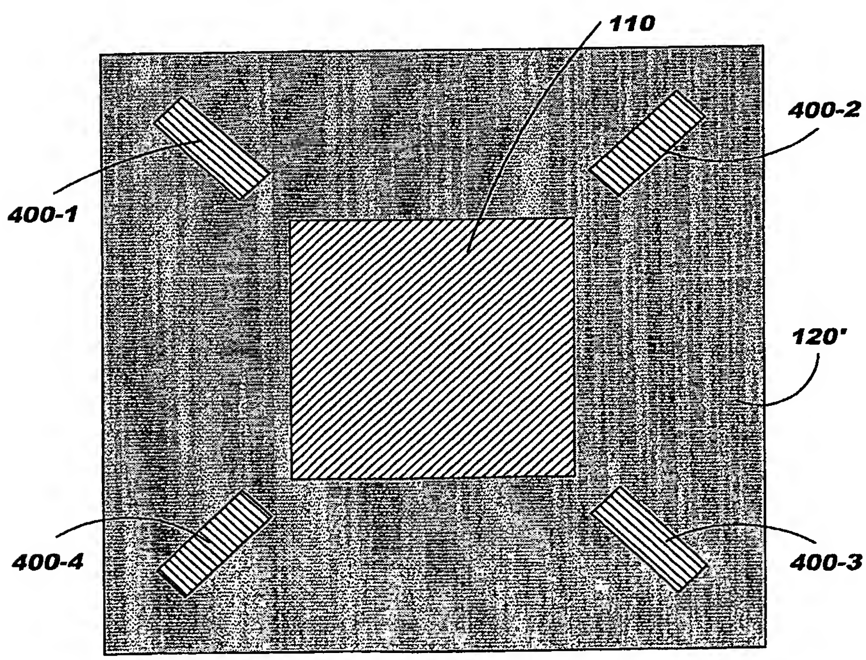

Figure 5

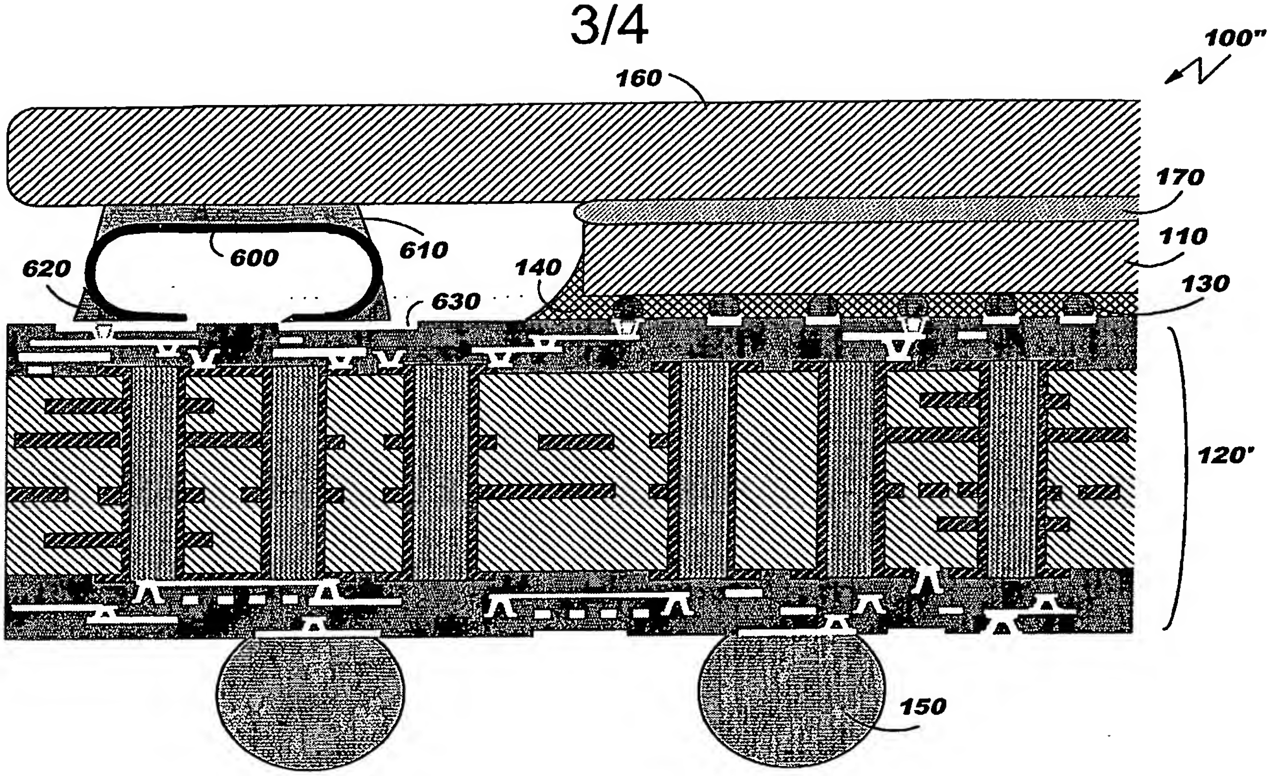

Figure 6

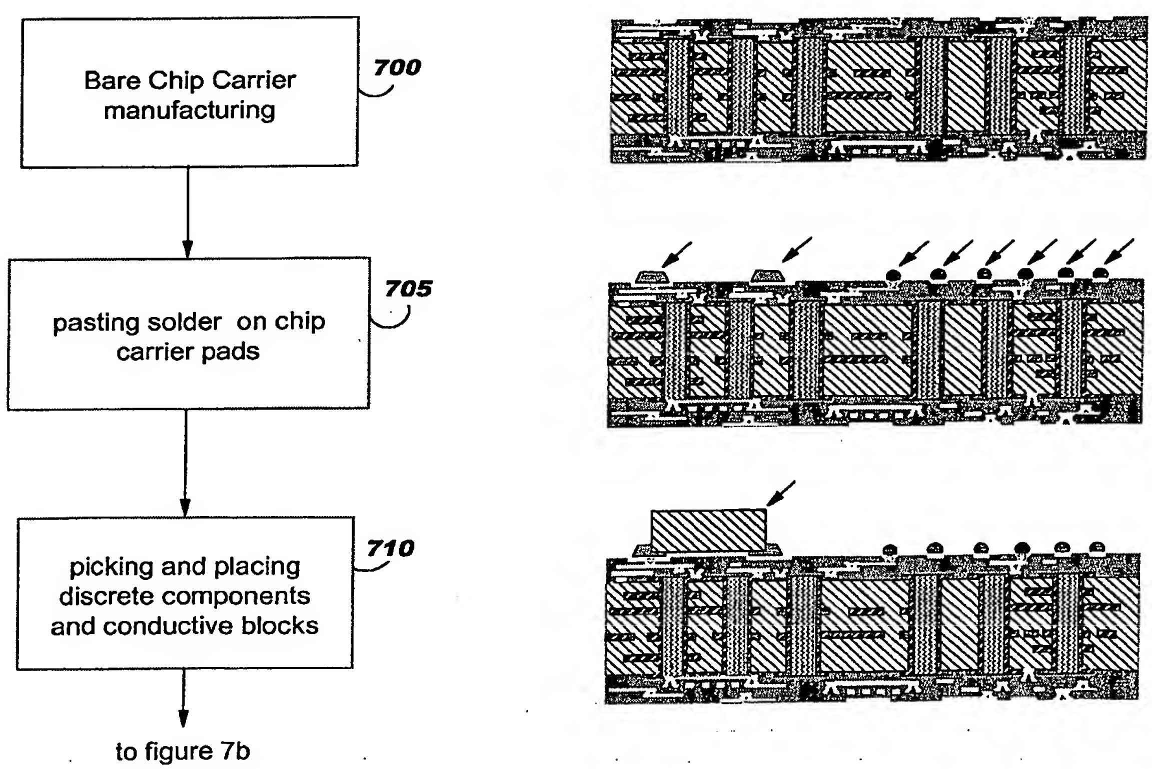

Figure 7a

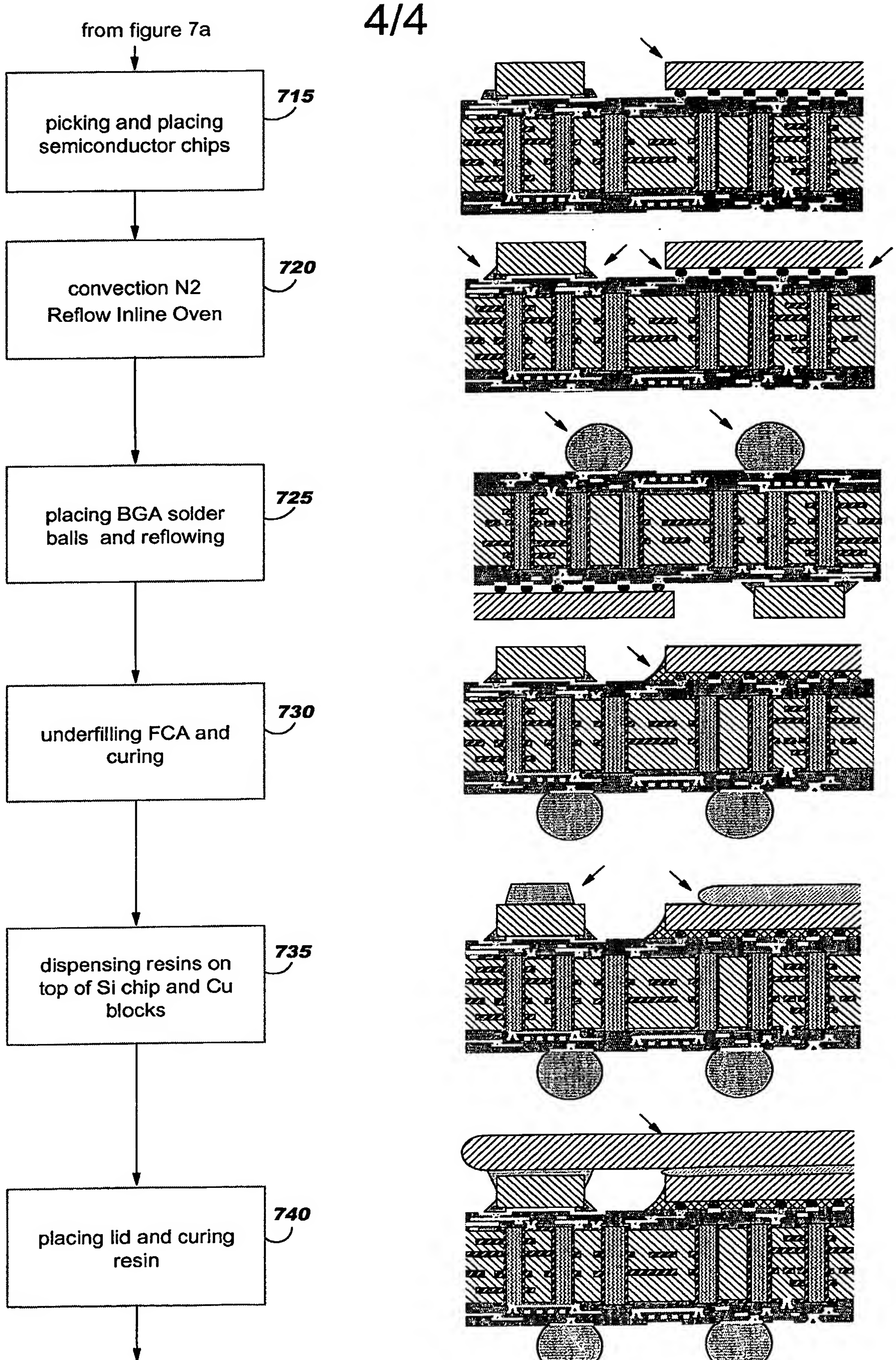
from figure 7a
picking and placing semiconductor chips
715
convection N2 Reflow Inline Oven
720
placing BGA solder balls and reflowing
725
underfilling FCA and curing
730
dispensing resins on top of Si chip and Cu blocks
735
placing lid and curing resin
740

Figure 7b